

Docket No.: M4065.0901/P901
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hagop A. Nazarian

Application No.: Not Yet Assigned

Confirmation No.:

Filed: Concurrently Herewith

Art Unit: N/A

For: SERIAL TRANSISTOR-CELL ARRAY
ARCHITECTURE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom. This Information Disclosure Statement accompanies the new patent application submitted herewith. A copy of each reference on PTO/SB/08 is attached.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter

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filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0901/P901. A duplicate copy of this paper is enclosed.

Dated: November 4, 2003

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Ryan H. Flax

Registration No.: 48,141

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorney for Applicant

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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Hagop A. Nazarian
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	M4065.0901/P901

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
		M. Durlam, et al., "A Low Power 1Mbit MRAM based on 1T1MTJ Bit Cell Integrated With Copper Interconnects", 2002 Symposium on VLSI Circuits Digest of Technical Papers; March 2, 2002.		
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		R. Butner, "Computing Unplugged", http://www.research.ibm.com/thinkresearch/pages/2001/20010202_mram.shtml ; visited 4/7/2003		

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